Delay Reduction in Three operand binary adder

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***Abstract*— Today's world places a high value on a processor's ability to operate its arithmetic logic units (ALU). The delay in processing an output is used to gauge the efficiency of the Arithmetic Logic Units (ALU). Addition is the fundamental operational unit of all arithmetic logic units (ALUs). So, using parallel prefix three operand binary adders, which are more efficient than other adders and the Propagator generator, which has a great delay performance, we have presented an addition technique in this study. The suggested adder outperforms the current three operand parallel prefix adder in terms of hardware efficiency (1.1534) and delay efficiency (1.07291).**

I. INTRODUCTION

Making a high speed parallel prefix three operand binary adder is the major goal of this paper. The three-operand binary adder is the fundamental functional component used in many cryptography and pseudo random bit generator (PRBG) techniques, as well as other applications, to carry out modular arithmetic. (Carry Save Adder), often known as CS3A, is the most popular technique for performing three-operand addition. The most commonly used parallel prefix three-operand binary adders are Brent-Kung adder, Ladner Fischer adder, propagator-generator adder are the most commonly used parallel algorithms.

Hybrid adder is the name of the proposed adder algorithm for a novel, high-speed three-operand adder. Using Very High Speed Hardware Description Language (VHDL), the proposed adder was created. It is simulated with the help of Altera Quarts II 8.0 which is an Electronic Design Automation tool. Thus the synthetization is verified for the performance in Altera ACEX1K:EP1K50TC0144-3. The results and the comparison have been discussed in the upcoming content.

II. WHAT IS THREE OPERAND BINARY ADDITION

The fundamental building block for carrying out all higher level to lower level operations is the three operand binary addition. (Han-carlson) adder is the fast and efficient method for adding two binary numbers in parallel. The operation of addition in Han Carlson adder is performed with involvement of two individual two operand additions. Even though this adder algorithm is considered to be a faster method in three operand addition. It is inefficient for higher bit rates as it is similar to that of an operating algorithm of basic ripple-carry adder(RCA).To overcome the above mentioned delay issues in the Han-Carlson adder various three operand binary addition and so on.

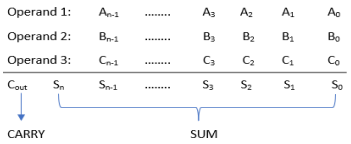

Fig 1. Modes of operation

III. BASIC ELEMENTS OF PARALLEL PREFIX ADDER

A. *Grey cell*

A grey cell is the fundamental block used in parallel prefix addition logic. And it consist of a AND and OR gate. It has one output and three inputs. It is a reusable part that, by permitting many instantiations in various designs, improves modularity and cuts down on design time. In general, grey cells are a crucial component of the VLSI design technique, allowing for the quick and efficient development of intricate integrated circuits.

$$G_{i:j} = G_{i:k}\,(OR)\,P_{i:k}\,(AND)\,G_{k-1:j}$$

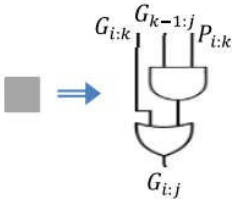

Fig 2(a). Grey cell

B. *Black cell*

A black cell is another functional building block in parallel prefix addition logic. And it consist of two AND gates and one OR gate. It is the combination of AND and OR gates. It has the pin configuration of four inputs and two outputs. It is the integrating of grey cell with a AND logic.

In which the output of AND logic is propagation index ($P_{i:j}$). And the output from the grey cell is generator ($G_{i:j}$).

$$G_{i:j} = G_{i:k}\ (OR)\ P_{i:k}\ (AND)\ G_{i:k-1:j}$$

$$P_{i:j} = P_{i:j}\ (AND)\ P_{k-1:j}$$

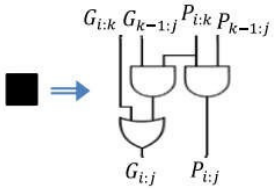

Fig 2(b). Black cell

IV. PARALLEL PRIFIX ADDER

The concept behind the prefix adder is parallel prefix computation, which includes creating prefix sums concurrently for a set of input data. The prefix adder computes the sum of two binary values in the case of addition by first producing a collection of partial sums and then merging them to yield the complete total. Prefix adders are superior to other types of adders in a number of ways, including quicker addition times and improved scalability for larger operands. It is frequently employed in high-performance arithmetic circuits, including those in microprocessors, digital signal processors, and other digital systems. The Ladner Fischer Adder, the Brent-Kung Adder, and the Propagator Generator are a few examples of prefix adders.

A. Ladner Fischer Adder

A quick way to add binary integers is to use the Ladner-Fischer adder, also referred to as the carry-skip adder. The system blocks the integers and adds separately inside each block. The calculation of the carry bits between the blocks is done in parallel, which cuts down on processing time. To avoid carry bits, the method uses block adders, a carry generator, and a carry skip network. This method expedites adding but necessitates more intricate circuitry.

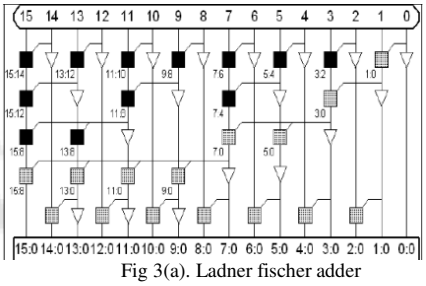

Fig 3(a). Ladner fischer adder

B. Brent-kung Adder.

Brent introduced Brent -Kung. Maximum logic depth is achieved by Brent-Kung adders, although they have few interconnects and little space. Create sums for even bit positions first, then for odd bit locations. It determines the prefix for groups, which is then used to determine the prefix for an 8-bit group, which is then used for a group of 16-bits and higher order words. The carry-in bits are then calculated by the affixes by tracking backwards at each level. Structured adders that resemble trees need 2log2n-1 stages. Black and grey cells are typically employed as buffers to lessen fan-out. This adder may be created for 23, 24, and 25-bit utilising CMOS logic and Transmission gates. The 16-bit Brent-Kung's structure is shown in the following image.

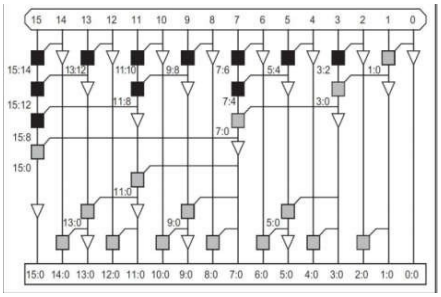

Fig 3(b). Brent-Kung adder

C. Propagator Generator

The propagation generator adder produces the necessary carry bits to finish the N-bit pair modulo-3 sums in parallel when used with a modulo-3 N-bit operand adder. Because of the logic structure's log2 3N operating levels, constant fan-in and fan-out designs are possible, as well as static precharge/discharge operation as opposed to fixed-rate precharge/discharge. The network can also be used as a conditional sum selection controller for a conditional sum adder in a simpler form.

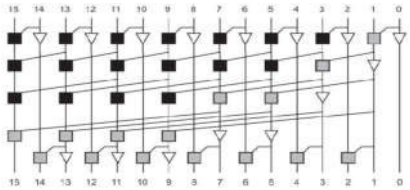

Fig 3(c). Propagation generator

V. PROPOSED ADDER

The proposed adder has the three operand parallel prefix adder in terms of optimizing hardware resources and improving the computation speed. Additionally, the incorporation of delay reduction techniques, including propagation delay optimization and gate-level optimizations, reduces the overall delay in the adder circuit. We proposed it has hybrid adder.

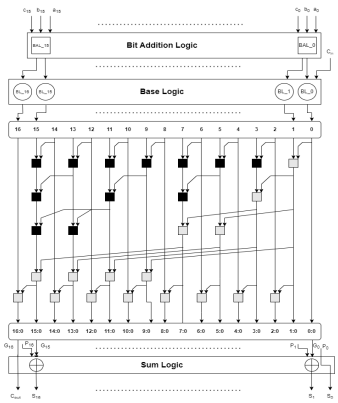

Fig 4. Proposed adder

Adder logic	Cell delay (ns)	Total delay (ns)
Brent Kung Adder	24.900	41.500
Ladner Fischer Adder	23.600	42.400
Propagator Generator Adder	20.600	34.100
Proposed Hybrid Adder	19.200	31.800

Table 1. Delay Comparison

The above Table (1) tells the delay comparison of existing and proposed adder.

VI. CONCLUSION

In conclusion, the design and implementation of an area-effective and reduced delay three-operand parallel prefix adder offer significant benefits in terms of optimizing hardware resources and improving computational speed. Through the application of area-effective techniques, such as resource sharing and compact circuit layouts, the adder can utilize available silicon area efficiently. Additionally, the incorporation of delay reduction techniques, including propagation delay optimization and gate-level optimizations, reduces the overall delay in the adder circuit. These optimizations enhance the performance of the adder, making it suitable for high-speed and low-power applications. The future scope of this research lies in exploring novel design techniques, power optimization, scalability, integration with advanced process technologies, and real-world applications. By continuing to advance the area-effective and reduced delay techniques, researchers can contribute to the evolution of digital circuits, leading to more efficient and high-performance computing architectures.

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